UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/551,843	09/27/2006	Tadahiro Ohmi	010986.56896US	5817

23911 7590 07/13/2007

CROWELL & MORING LLP
INTELLECTUAL PROPERTY GROUP
P.O. BOX 14300
WASHINGTON, DC 20044-4300

EXAMINER	
WITHERS, GRANT S	
ART UNIT	PAPER NUMBER
2812	
MAIL DATE	DELIVERY MODE
07/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/551,843	OHMI ET AL.	
	Examiner	Art Unit	
	Grant S. Withers	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

WALTER LINDSAY JR.
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/03/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Application filed on 09/27/2006.

Currently, claims 1-20 are pending.

Priority

1. Acknowledgment is made of applicant's claim for priority to PCT JP2004/004700.

Information Disclosure Statement

The information disclosure statement filed 10/03/2005 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because reference AF has no accompanying copy, or English translation, and is not retrievable by the examiner. Reference AF has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Specification

2. A substitute specification in proper idiomatic English and in compliance with 37 CFR 1.52(a) and (b) is required. The substitute specification filed must be accompanied by a statement that it contains no new matter.

Claim Objections

3. Claim 8 is objected to because of the following informalities: on line 2, "claim" is misspelled. The suggested change is to spell "claime" as "claim".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-9 and 11-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Inoue et al. (US 2004/0031985, dated 02/24/2003).

As to claim 1, Inoue et al. shows (See Fig. 8-11) a semiconductor device comprising:

a silicon substrate;

a gate electrode layer (GE 6; Fig 11; page 3, [0042]); and a gate insulation film (portion of insulation film 5 right below the topmost layer of atoms in the layer, and above the first layer of atoms of the layer; Fig. 9; page 3, [0038]) disposed between the silicon substrate and the gate electrode layer 6, wherein

the gate insulation film 5 is a high relative permittivity (high-k) film (polysilicon nitride having a relatively high k value; Fig. 10; page 3, [0038]) being

formed by performing a nitriding (nitriding; Fig. 10; page 3, [0038]) treatment on a mixture of a metal and silicon (the bottom portion of layer 5, which is formed below the middle portion of layer 5; Fig. 10; page 3, [0038]).

As to claim 2, Inoue et al. shows a semiconductor device according to claim 1 above, wherein the gate insulation film 5 is formed according to a plasma CVD technology (first the layer 5 is formed by CVD, and then further processed by plasma, in a plasma CVD technology; page 3, [0037] and [0038]).

As to claim 3, Inoue et al. shows a semiconductor device according to claim 1 above, wherein a silicon nitride film (bottom portion of layer 5; Fig. 10; page 3, [0038]) is formed as a barrier layer (i.e. layer presenting a barrier to electrons) between the silicon substrate and the gate insulation film (middle portion of 5).

As to claim 4, Inoue et al. shows a semiconductor device according to claim 3 above, wherein the silicon nitride film (bottom portion of layer 5) is formed according to a direct nitriding technology by plasma (nitriding by plasma; Fig. 10; page 3, [0038]).

As to claim 5, Inoue et al. shows a semiconductor device according to claim 1 above, wherein a silicon nitride film (top portion of layer 5; Fig. 10, page 3, [0038]) is disposed on the gate insulation film (middle portion of layer 5).

As to claim 6, Inoue et al. shows a semiconductor device according to claim 5 above, wherein the silicon nitride film (top portion of layer 5) and the gate

insulation film (middle portion of layer 5) are alternately (i.e. one after another) laminated (i.e. formed or set in thin layers) on the silicon substrate.

As to claim 7, Inoue et al. shows a semiconductor device according to claim 1 above, wherein a buffer layer (lower portion of layer 5) is formed between the silicon substrate and the gate insulation film (middle portion of layer 5).

As to claim 8, Inoue et al. shows a semiconductor device according to claim 1 above, wherein an alumina (Al_2O_3) monocrystal film (Al_2O_3 layer 15; Fig. 8; page 3, [0036]) is formed between the silicon substrate and the gate insulation film (middle portion of layer 5).

As to claim 9, Inoue et al. shows a semiconductor device according to claim 8 above, wherein the alumina monocrystal film 15 is formed according to a plasma CVD technology (MOCVD; Fig. 8; page 3, [0036]).

As to claim 11, Inoue et al. shows a method for manufacturing a semiconductor device comprising the steps of:

forming a gate insulation film (middle part of layer 5; Fig. 10; page 3, [0038]) which is a high relative permittivity (high-k) film (layer 5 having a relatively high k compared to copper; Fig. 10; page 3, [0038]) by performing a nitriding treatment (nitriding; Fig. 10; page 3, [0038]) on a mixture of a metal and silicon (bottom portion of layer 5; Fig. 10; page 3, [0038]); and

forming a gate electrode 6 layer on the gate insulation film (middle portion of layer 5).

As to claim 12, Inoue et al. shows a method for manufacturing a semiconductor device according to claim 11 above, wherein the gate insulation film (middle portion of layer 5) is formed according to a plasma CVD technology (first the layer 5 is formed by CVD, and then further processed by plasma, in a plasma CVD technology; page 3, [0037] and [0038]).

As to claim 13, Inoue et al. shows a method for manufacturing a semiconductor device according to claim 11 above, further comprising the step of forming a silicon nitride film (bottom portion of poly nitride layer 5; Fig. 10; page 3, [0038]) as a barrier layer (a barrier for electrons) between the silicon substrate and the gate insulation film (middle portion of layer 5).

As to claim 14, Inoue et al. shows a method for manufacturing a semiconductor device according to claim 13 above, wherein the silicon nitride film is formed according to a direct nitriding by plasma.

As to claim 15, Inoue et al. shows a method for manufacturing a semiconductor device according to claim 11 above, wherein a silicon nitride film (top portion of layer 5; Fig. 10; page 3, [0038]) is disposed on the gate insulation film (middle portion of layer 5).

As to claim 16, Inoue et al. shows a method for manufacturing a semiconductor device according to claim 15 above, wherein the silicon nitride film (top portion of layer 5; Fig. 10; page 3, [0038]) and the gate insulation film (middle portion of layer 5) are alternately laminated on the silicon substrate.

As to claim 17, Inoue et al. shows a method for manufacturing a semiconductor device according to claim 11 above, further comprising the step of forming a buffer layer (lower portion of layer 5) between the silicon substrate and the gate insulation film (middle portion of layer 5).

As to claim 18, Inoue et al. shows a method for manufacturing a semiconductor device according to claim 11 above, further comprising the step of forming an alumina ($A1_2O_3$) monocrystal film (Al_2O_3 layer 15; Fig. 8; page 3, [0036]) between the silicon substrate and the gate insulation film (middle portion of layer 5).

As to claim 19, Inoue et al. shows a method for manufacturing a semiconductor device according to claim 18 above, wherein the alumina monocrystal film 15 is formed according to a plasma CVD technology (MOCVD; Fig. 8; page 3, [0036]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (US 2004/0031985, dated 02/24/2003) as applied to claims 1 and 11 above, and further in view of Huppertz et al. (Huppertz, Hubert $Ba_2Nd_7Si_{11}N_{23}$ – A

Nitridosilicate with a Zeolite-Analogous Si – N Structure, Angew. Chem. Int. Ed. Engl. 1997, Vol. 36, No. 23, pg. 2651-2).

As to claim 10, Inoue et al. shows a method for manufacturing a semiconductor device according to claim 1 above.

As to claim 20, Inoue et al. shows a method for manufacturing a semiconductor device according to claim 11 above.

However, pertaining to claim 10, Inoue et al. fails to show a semiconductor device according to claim 1 above, wherein the gate insulation film has one of compositions selected from a following list:

$M_3Si_6N_{11}$ (M=La, Ce, Pr, Nd, Sm);

$M_2Si_5N_8$ (M=Ca, Sr, Ba, Eu);

$MYbSi_4M_7$ (M=Sr, Ba, Eu);

$BaSi_4N_7$;

$Ba_2Nd_7Si_{11}N_{23}$.

Also, pertaining to claim 20, Inoue et al. fails to show a method for manufacturing a semiconductor device according to claim 11 above, wherein the gate insulation film has one of compositions selected from a following list:

$M_3Si_6N_{11}$ (M=La, Ce, Pr, Nd, Sm);

$M_2Si_5N_8$ (M=Ca, Sr, Ba, Eu);

$MYbSi_4M_7$ (M=Sr, Ba, Eu);

$BaSi_4N_7$;

$Ba_2Nd_7Si_{11}N_{23}$.

In the same field of endeavor, Huppertz et al. teach a method of forming $Ba_2Nd_7Si_{11}N_{23}$ (synthesis of $Ba_2Nd_7Si_{11}N_{23}$; not shown; page 2651, column 2, [0007]).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to have used the method of forming $Ba_2Nd_7Si_{11}N_{23}$ layers as taught in Huppertz et al., to have made the insulating film in Inoue et al. with the motivation that doing so would form a highly stable oxide film (high stability; not shown; page 2651, [0005]) as an insulating film. The reasonable expectation of success results from the method of forming $Ba_2Nd_7Si_{11}N_{23}$ as taught by Huppertz et al. being well known in the art to form stable insulating layers as in Inoue et al.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ohmi (US 4,907, 053, patented 03/06/1990) shows a method of depositing a nitride layer as an insulating layer on a silicon substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Grant S. Withers whose telephone number is (571)-270-1570. The examiner can normally be reached on Mon-Thurs 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571)-272-1873. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GSW
07/03/2007

WALTER LINDSAY JR.
PRIMARY EXAMINER